High Resolution Spectroscopy System for Eurisys Segmented Clover Detectors[1]

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Abstract

The data acquisition system for a Eurisys segmented Clover germanium detector is described with special emphasis placed on the system architecture and experimental results. The CAMAC-based module consists of four high-resolution quasi-triangular shaping amplifiers with accompanying timing filter amplifiers and constant-fraction discriminator circuits. Both time and energy signals are digitized for the four high resolution channels. Three shaping amplifiers process the side channel signals which are digitized with a 12-bit converter. Signals from an 8-channel BGO card included for Compton suppression are used to veto a clean germanium signal in the trigger logic board. Threshold voltages as well as logic commands in the unit are controlled via a CAMAC interface chip, and readout is accomplished via a front panel FERABUS readout architecture. Both analog and digital signals are multiplexed to the front panel for inspection. Details of the design and experimental results are presented.

I. INTRODUCTION

Increased detection efficiency for Ge gamma-ray detectors requires larger-volume crystals of hyper-pure Ge. One cost-effective way of achieving this is by combining several smaller crystals into one large detector. For example, EURISYS manufacture "clover" detectors by mounting four Ge crystals in one cryostat, side-by-side in a geometry reminiscent of a four-leaf clover. These detectors may also be electronically segmented to provide enhanced position/angular information. In addition, improved peak-to-total ratio can be achieved by surrounding the Ge detector by a BGO anti-Compton shield, used to veto events where the gamma-ray scatters out of the Ge into the BGO.

A dozen or more such Compton-suppressed, segmented clover detectors may be assembled into large detector arrays, such as the CLARION array at ORNL. Such an array requires a large quantity of electronics; the eleven CLARION clover detectors require 44 channels of high-resolution shapers, ADCs, TFAs, CFDs and TDCs, 33 low-resolution shapers and ADCs, 88 channels of BGO discrimination and Compton-suppression logic, some BGO shapers, ADCs and TDCs, readout hardware and control, etc. Such a quantity of electronics in conventional modular NIM/CAMAC/VME format would be both bulky and expensive.

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II. SYSTEM ARCHITECTURE

A. High Resolution Shaper Amplifiers

As shown in the system block diagram of Figure 1, the high resolution shaper boards receive signals from the preamplifiers located in the base of the Clover assemblies. A coarse gain adjust under CAMAC control sets the range at 4- or 8-MeV full scale. The energy signal is processed with an 8-stage quasi-triangular shaper having a shaping index of 4.2 µs and includes a baseline restorer circuit. Timing signals from the zero-crossing of the bipolar shaped pulses are used to generate the ADC convert pulse at the signal peak. The CFD threshold and walk adjustments are set for each channel *via* CAMAC control. A pile-up mode setting either inhibits conversion in the presence of pile-up or sets a flag in the 15^{th} data bit to indicate pile-up.

B. Side Channel Amplifiers

The three side channel amplifiers include two modified bridged-T filter sections followed by a passive low pass filter stage with an overall shaping index of 3.3 µs. The baseline restorer circuit and the peak convert signal are gated when the signal level exceeds the threshold set by one of the CAMAC-controlled DAC voltages.

C. 8-Channel BGO Processor

Eight identical fast timing amplifiers with comparators generate an 8-fold hit pattern which is subsequently read out indicating which channels had events exceeding thresholds as set by eight separate CAMAC-controlled DAC voltages. The eight time-over-threshold logic signals are ORed to form a BGOHIT signal which is used in the trigger logic card to veto the CLEAN Ge signal. The BGOHIT signal is also delayed by 1µs and used to generate the STOP signal for the BGO TDC channel. The eight BGO input signals are summed and shaped to provide an analog signal for the BGO ADC; the ADC convert signal and a simple baseline restorer circuit are also implemented.

D. ADCs

The 14-bit ADCs were patterned closely after the units designed for the Gammasphere project using a Gatti method to improve the differential nonlinearity [1]. Special test fixtures were constructed to measure and calibrate the gain and offsets and to match the gain of the Gatti subcircuit by observing a histogram of 256 successive digitizations of a fixed value.

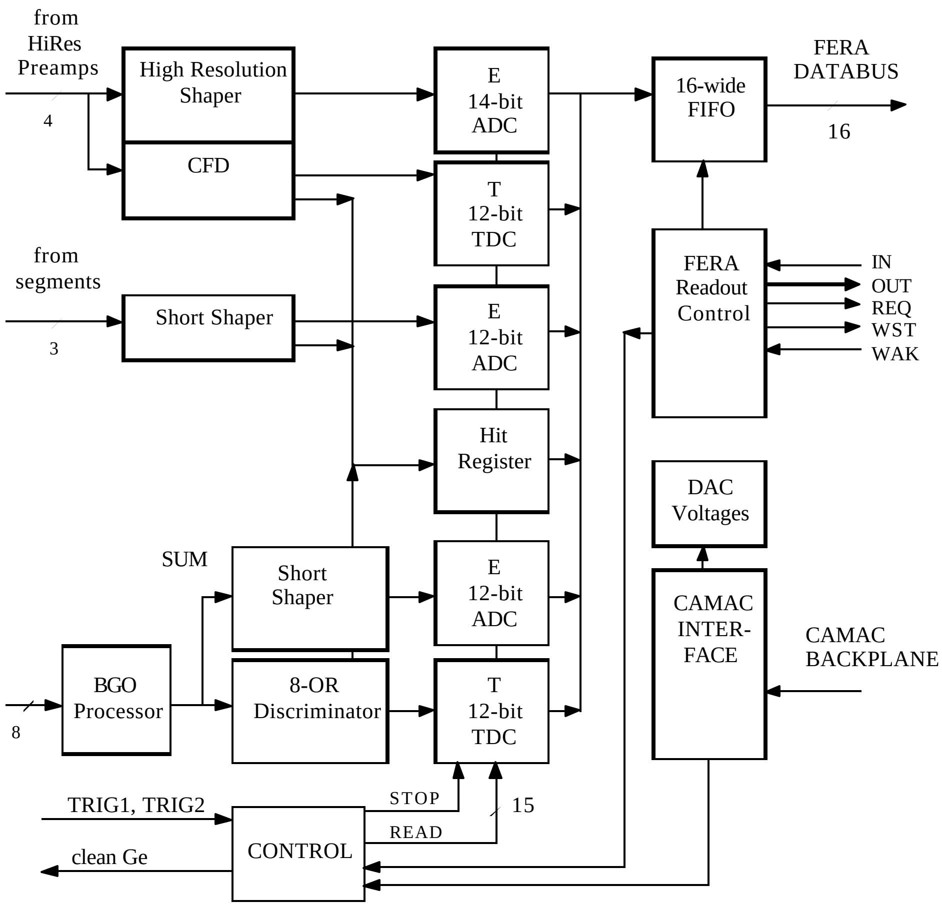

Figure 1: Clover Electronics Module block diagram.

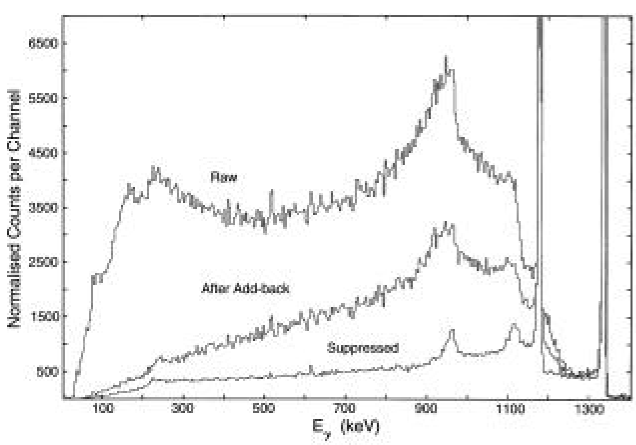

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Figure 2. The spectrum of ^{60}Co measured before and after add-back and with suppression.

III. EXPERIMENTAL RESULTS

Twelve Clover modules have been built and tested both independently and with up to 12 units connected through a daisy-chained FERABUS readout. Figure 2 illustrates the high peak-to-total ratio exhibited in early testing. Current requirements for the $\pm$12-volt supply lines were +750 and –800 mA respectively due largely to the four high resolution shaping boards at +74 and –67.5 mA each.

Modifications were made to the trigger logic card, the TAC operation, and the FERABUS readout logic chip during operational checkout of the module. The trigger logic card receives four CFD signals from the Germanium high resolution cards. Each signal path is delayed by 100-ns to 200-ns under DAC control to align the respective timing of the four channels. An 8-fold OR of the BGO signals is also brought to the trigger logic card to veto a clean Germanium event. The BGO logic pulse is stretched to at least 400 ns and precludes a clean germanium signal from initiating further digitization. Front panel current signals indicating a clean Ge event or a BGO event are available for external trigger logic processing. A TRIG1 logic pulse must be received back to the module within 1μs to process the event. The TRIG1 logic pulse serves as the stop for the BGO timing logic and initiates the storage of the hit pattern logic from the BGO channels. The range of the four high resolution timing channels was modified from 1 to 5 μs to allow for longer coincidence times with other detectors in the system. The TRIG2 logic pulse established the stop signal for these four timing channels while each respective CFD initiated the start of the TAC signal.

The FERABUS readout logic chip receives a token from its adjacent neighbor and places a 16-word packet on the differential ECL bus and then passes the token to its downstream neighbor. Readout time for each 16-bit word was set at approximately 120-ns for a total module readout time of just under 2 μs. The first word in the readout includes a header word with an 8-bit serial number downloaded to each module under CAMAC control during the setup. Other words include a hit pattern for the module, 4 high resolution energy values, 4 high resolution timing values 3 side channel energy values, and both energy and timing information for the summed BGO channels. The FERABUS chip was implemented using a Xilinx XC9572 FPGA which was programmable *in situ*. Token passing was redefined so that in the event an ADC conversion was in process, the token was held until conversion was completed before passing it along to neighboring modules.

IV. References

[1] B. T. Turko *et al*., "A High Resolution 14-bit ADC for Gammasphere Project," *Lawrence Berkeley Laboratory Report LBL-32246*, October 1992.